AMENDMENTS TO THE CLAIMS

1-8. (Canceled).

9. (Currently Amended) A method for conducting a multiple word line selection test on a semiconductor memory device provided with a plurality of memory cell blocks, which include a first memory cell block and a second memory cell block, each of the memory cell blocks having a plurality of memory cells and a plurality of word lines connected to the memory cells, and a plurality of sense amp groups connected to the first and second memory cell blocks, each of the sense amp groups amplifying cell information read from the plurality of memory cells of an associated one of the memory cell blocks, and a plurality of block control circuits respectively connected to the plurality of memory cell blocks, which include a first block control circuit and a second block control circuit, wherein when the multiple word line selection test is conducted, the plurality of word lines and the sense amp group in each of the plurality of memory cell blocks are activated, the method comprising:

a first step for generating a first reset signal using the first block control ~~unit~~ circuit;

a second step for inactivating multiple word lines in the first memory cell block and the sense amp group associated with the first memory cell block in response to the first reset signal; and

a ~~second~~ third step for generating a second reset signal using the second block control ~~unit~~ circuit;

a ~~third~~ fourth step for inactivating multiple word lines in the second memory cell

block and the sense amp group associated with the second memory cell block after performing the first step in response to the second reset signal.

10. (Original) A method for conducting a multiple word line selection test on a semiconductor memory device provided with a plurality of memory cell blocks, which include a first memory cell block and a second memory cell block, each of the memory cell blocks having a plurality of memory cells and a plurality of word lines connected to the memory cells, and a plurality of sense amp groups connected to the first and second memory cell blocks, each of the sense amp groups amplifying cell information read from the plurality of memory cells of an associated one of the memory cell blocks, the method comprising:

a first step for activating one of the plurality of word lines in the first memory cell block and activating the sense amp group associated with the first memory cell block after a predetermined time;

a second step for activating word lines other than the one that has been activated in the first memory cell block;

a third step for activating one of the plurality of word lines in the second memory cell block and activating the sense amp group associated with the second memory cell block after a predetermined time;

a fourth step for activating word lines other than the one that has been activated in the second memory cell block;

a fifth step for inactivating multiple word lines in the first memory cell block and the

sense amp group associated with the first memory cell block; and

a sixth step for inactivating multiple word lines in the second memory block and the sense amp group associated with the second memory block after performing the fifth step;

wherein the third and fourth steps are performed while the first and second steps are continuously performed or the second and fourth steps are performed while the first and third steps are continuously performed.

11. (Previously Presented) A semiconductor memory device comprising:

a plurality of memory cell blocks, wherein each of the memory cell blocks includes a plurality of memory cells and a plurality of word lines connected to the memory cells;

a plurality of row decoders connected to the plurality of memory cell blocks, wherein each of the row decoders selects one of the word lines in an associated one of the memory cell blocks;

a plurality of sense amp groups connected to the plurality of memory cell blocks, wherein each of the sense amp groups amplifies cell information read from the plurality of memory cells of an associated one of the memory cell blocks;

a plurality of block control circuits connected to the plurality of row decoders, wherein each of the block control circuits simultaneously selects multiple word lines in an associated one of the memory cell blocks and generates a sense amp control signal and a word line reset signal; and

a plurality of sense amp drive circuits connected to the plurality of block control circuits and the plurality of sense amp groups, wherein each of the sense amp drive circuits

selectively activates an associated one of the sense amp groups based on the sense amp control signal of the associated one of the block control circuits, each of the sense amp drive circuits including a latch circuit that is reset by the word line reset signal and a sense amp reset timing signal.

12. (Original) The device according to claim 11, further comprising:

a timing signal generation circuit connected to the plurality of sense amp drive circuits for generating a sense amp set timing signal, which selectively controls activation of the plurality of sense amp groups, and a sense amp reset timing signal;

wherein the latch circuit receives the sense amp set timing signal and the sense amp reset timing signal.

13. (Original) The device according to claim 11, wherein the block control circuit includes a word line reset signal generation circuit for generating a word line reset signal that stops selecting the plurality of word lines, wherein the latch circuit receives the word line reset signal including block information.